

Substitute for Form 1449 A & B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	Cont. of Serial No. 09/425,886	
			Confirmation Number	Not Yet Assigned	
			Filing Date	June 24, 2003	
			First Named Inventor	Pranav ASHAR et al.	
			Art Unit	Not Yet Assigned 2133	
Examiner Name	Not Yet Assigned ABRAHAM				
Attorney Docket Number	A8612				
Sheet	2	of	2		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		Number	Kind Code ² (if known)		

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)			

OTHER ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation ⁶
EA		SETOVICH, E., et al. "Sequential Circuit Design Using Synthesis and Optimization", Proceedings of ICCD, 1992	
EA		GUPTA, A., ASHAR, P., "Integrating a Boolean Satisfiability and BDDs for Combinational Verification, Proceedings of VLSI Design 98, pp. 222-225, 1998	
EA		BURCH, J. and SINGHAL, V., "Tight Integration of Combinational Verification Methods", Proceedings of ICCAD, pp. 570-576, 1978	
EA		TOMITA, M., SUGANUMA, N., and HIRANO, K., "Pattern generation for locating logic design errors", IEICE Transactions Fundamentals, vol. E77-A, 1994	

Examiner Signature	ESQW Abraham	Date Considered	06/24/04
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<u>EA</u>		US 5,831,996		11/03/1998	Abramovici et al.		
<u>EA</u>		US 6,086,626		07/11/2000	Jain et al.		
<u>EA</u>		US 6,138,266		10/24/2000	Ganesan et al.		
<u>EA</u>		US 5,909,374		06/01/1999	Matsunaga		
<u>EA</u>		US 6,026,222		02/15/2000	Gupta et al.		
<u>EA</u>		US 6,247,163	B1	06/12/2001	Burch et al.		
<u>EA</u>		US 5,754,454		05/19/1998	Pixley et al.		
<u>EA</u>		US 5,506,852		04/09/1996	Chakradhar et al.		
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<u>EA</u>		ABADIR, M., FERGUSON, J., KIRKLAND, Thomas E. "Logic Design Verification via Test Generation"; IEEE Transactions on Computer Aided Design, vol. 7, no. 1, pp. 138-148, January 1988					
<u>EA</u>		BRYANT, R., "Graph-Based Algorithms for Boolean Function Manipulation, IEEE Transactions On Computer, C-35(8): 677-691, August 1996					
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<u>EA</u>		JAIN, J., MUKHERJEE, R., FUJITA, M., "Advanced Verification Techniques Based On Learning" Proceedings of DAC, June 1995					
<u>EA</u>		KUEHLMANN, A., CHENG, D., SRINIVASAN, A., LAPOTIN, D.: "Error Diagnosis for Transistor-Level Verification", Proceedings of DAC, pp. 218-223, 1994.					
<u>EA</u>		KUKIMOTO, Y., FUJITA, M., "Rectification Method for Lookup-Table Type FPGA's Proceedings of ICCAD, pp. 54-61, 1992					
<u>EA</u>		MADRE, J., COUDERT, O., and BILLON, P., "Automating the Diagnosis and the Rectification of Design Errors with PRIAM", Proceedings of ICCAD, pp. 30-33, 1989					
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<u>EA</u>		SILVA, J., SAKALLAH, K., "GRASP -- A New Search Algorithm for Satisfiability, Proceedings of ICCAD, pp. 220-227, 1996					
<u>EA</u>		TAMURA, K., "Locating Functional Errors in Logic Circuits" Proceedings of ICCAD, pp. 468-471, November 1989					
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<u>EA</u>		WATANABE, Y., BRAYTON, R., "Incremental Synthesis for Engineering Changes", Proceedings of ICCAD, pp. 40-43, 1991					
<u>EA</u>		HAUNG, S., CHEN, K.C., CHENG, K.T., "Error Correction Based on Verification Techniques", Proceedings of DAC, pp. 258-261, 1996					
Examiner Signature		<u>SSAW Abreha</u>			Date Considered	<u>06/25/04</u>	

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